After the claims, please add the following Abstract section:

Abstract of the Disclosure

An embodiment of this invention pertains to a system and method for balancing memory accesses to a low cost memory unit in order to sustain and guarantee a desired line rate regardless of the incoming traffic pattern. The memory unit may include, for example, a group of dynamic random access memory units. The memory unit is divided into memory channels and each of the memory channels is further divided into memory lines, each of the memory lines includes one or more buffers that correspond to the memory channels. The determination as to which of one or more buffers within a memory line an incoming information element is stored is based on factors such as the number of buffers pending to be read within each of the memory channels, the number of buffers pending to be written within each of the memory channels, and the number of buffers within each of the memory channels that has data written to it and is waiting to be read.

NE must be on separate page

In the Claims:

Please add the following claims:

1. (new) A method to optimally access a memory unit where the memory unit is logically partitioned to form a plurality of memory channels, the plurality of memory channels are further logically partitioned to form a plurality of memory lines, each of the plurality of memory lines includes a plurality of buffers and each of the plurality of buffers corresponds to a separate one of the plurality of memory channels, comprising:

determining at least one load value of each of the plurality of memory channels; and

based on the determined at least one load value, selecting a particular one of the plurality of memory channels.